IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/817,548
Filing Date ..... April 2, 2004
Inventor ..... Martin Ceredig Roberts et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2814
Examiner ..... Peralta, Ginette
Attorney's Docket No. MI22-2550
Title: Methods of Forming Capacitors, and Methods of Forming DRAM Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

The attached Form PTO/SB/08a is submitted in compliance with 37 CFR §1.56. Pursuant to FEDERAL REGISTER, Vol. 69, No. 182, pg. 56542 (September 21, 2004), no copies of any cited U.S. patents or U.S. published applications are included herewith. Copies of all other cited art are attached. No admission is made regarding whether the listed references are prior art.

Citation of the referenced art is respectfully requested.

Respectfully submitted,

Dated: December 15, 2005

By: Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

EV633202625

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	11/168,697
Filing Date	June 27, 2005
First Named Inventor	Arup Bhattacharyya
Art Unit	2815
Examiner Name	Lee, Eugene
Attorney Docket Number	MI22-2911

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US- 6,222,215	04-2001	Zahurak	
	2	US- 6,121,653	09-2000	Juengling	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
	3	DE4213945A1	11-05-1992			

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

EV633202625

CLIPPEDIMAGE= DE004213945A1
PUB-NO: DE004213945A1
DOCUMENT-IDENTIFIER: DE 4213945 A1
TITLE: Memory capacitor in semiconductor device for DRAM cells - comprises
conductively doped poly:silicon@ layers and insulating layer comprising capacitor dielectric adjacent to memory node of 2nd poly:sil
PUBN-DATE: November 5, 1992
INVENTOR-INFORMATION:

NAME	COUNTRY
FAZAN, PIERRE	US
CHAN, HIANG C	US

ASSIGNEE-INFORMATION:

NAME	COUNTRY
MICRON TECHNOLOGY INC	US

APPL-NO: DE04213945
APPL-DATE: April 28, 1992
PRIORITY-DATA: US69285991A (April 29, 1991)
INT-CL_(IPC): H01L021/72; H01L027/108
EUR-CL (EPC): H01L027/108
US-CL-CURRENT: 257/307

ABSTRACT:
A memory capacitor has (1) a conductively doped first polysilicon layer with a
first and a second end, the first end making contact with a memory node connection of an access device and the second end being insulated from an adjacent conductive material by a dielectric; (2) a conductively doped second polysilicon layer adhering to the first polysilicon layer, forming a memory node plate of I-shaped cross-section; (3) an insulating layer comprising a capacitor dielectric adjacent to the memory node plate and extending the same

distance as the latter except for regions for the contact point at its first end and the insulation at its second end; and (4) a conductively doped third polysilicon layer forming a cell palte which has an upper and a lower surface, and adjacent to and of the same extent as the capacitor dielectric layer. The
doped polysilicon is pref. produced by gas-phase deposition, as are all the dielectric layers. The capacitor dielectric layer is selected form nitrides, oxidised nitrides, Ta2O5, oxidised Ta2O5 and SrTiO3. USE/ADVANTAGE - Used in
the mfr. of DRAM, VRAM and other stacked memory cell devices. Capacitor maximises the memory cell active surface in the prodn. of high-density DRAMs
(an increase of 200% or more is quoted).